Intel® I/O Controller Hub 6 (ICH6) Family

Specification Update

May 2005

Notice: The ICH6 Family product may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 301474-011

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Revision History

Revision	Description	Date
1.0	Initial Release.	June 2004
2.0	Modified: Erratum 3-SATA Swap Bay Device Detection, 7-Intel ICH6 Completion Delays Documentation Changes 1-PCI Device Register ID Table updated for B2 stepping. Added: Erratum: 9-Intel ICH6 PCI Express* Completion Timer Not Halting in L1, 10-Intel ICH6 Does Not Send Minimum Number TS2 on PCI Express*, 11-Intel ICH6 PCI Express* Recovery, 12-Intel ICH6 PCI Express* Extended Tag Capability Bit Specification Changes: 1-AHCI SALP Bit Change, 2-V_{IL14} Change Specification Clarifications: 1-IDE Controller Interrupt Status Note Documentation Changes: 2-Input Signal Association Table Correction	August 2004
3.0	Added: Erratum: 13-ICH6 Does Not Ignore a PCI Express* Null Packet, 14-ICH6 PCI Express DLLPs With Unknown Encoding Type, 15-SATA SRST During Link Low Power States Specification Changes: 3-XOR Test Change Specification Clarifications: 2-Table 22-20 Note Corrections, 3-Standard ATA Emulation Clarification, 4-Secondary PCI Bus Reset, 5-EHCI Test Mode Documentation Changes: 3-DC Current Characteristics Table Update	September 2004
4.0	Added: Errata: 16-PCI Express Replay, 17-ICHR/RW SATA FIS Posting Cycle, 18-USB Output Voltage Specification Changes: SIR28 Change Specification Clarifications: 6-IRQ14/IRQ15 and SERIRQ, 7-t302 Clarification	October 2004
5.0	Added: New Component Marks Errata: Errata: 19-ICH6 AHCI Command FIS SYNC Escape, 20-ICH6 ACHI PxCMD.CR Bit, 21-ICH6 High Definition Audio Payload Capabilities Registers, 22-ICH6 PIO Setup FIS Error, 23-ICH6 PCI Express Surprise Removal Specification Changes: 5-Intel Wireless Connect Technology/ICH6W/ICH6RW Defeature, 6-EE_SHCLK Change, 7-INIT3_3V VOL Change Specification Clarifications: 8-EDD (Execute Device Diagnostics) Command Completion Clarification, 9-SMBus Reset Clarification Documentation Changes: 4-AHCI CAP Default Correction, 5-LCTL Corrections Modified: Removed Intel Wireless Connect Technology references	November 2004
6.0	Added: Specification Changes: 8-t214 Change, 9-Peer Cycle Change Documentation Changes: 6-PxSSTS.IPM Correction	December 2004

Revision	Description	Date
7.0	Moved all Specification Changes, Specification Clarifications and Documentation Changes into parent Datasheet (301473-002). Modified: Errata: 11-PCI Express Recovery Documentation Changes: 1-PCI Device Revision ID Added: ICH6/ICH6-M Marks Errata: 24-PCI Express Scrambling, 25-AHCI PxSERR:[M] Bit, 24-L0s With Extended Sync, 25-ICH6-M DPRSLPVR.	January 2005
8.0	Added: Errata: 28-PATA V-Threshold, 29-PCI Express SKP/InitFCx Contention, 30-DMI L0s Latency Bit Attribute, 31-PCI Express Two DWord Malformed TLP	February 2005
9.0	Moved the following to the parent ICH6 Family Datasheet (301473-002): Errata: 28-PATA V-Threshold, 29-PCI Express SKP/InitFCx Contention, 30-DMI L0s Latency Bit Attribute, 31-PCI Express Two DWord Malformed TLP Added: Errata: 32-Full-speed USB ISOC End of Packet, 33-ICH6R/ICH6-M AHCI SATA Interlock Switch. Specification Clarifications: 1-t216 Clarification, 2-C2 Support, 3-LPC Cycle Clarification. Document Changes: 2-CAP.SALP, 3-Memory Address Range Addition, 4-D30:F0.PSTS Correction.	March 2005
10.0	Modified: Erratum: #11-PCI Express Recovery, #14-Intel(R) ICH6 PCI Express DLLPs with Unknown Encoding Type Documentation Changes: #1-PCI Device Revision ID. Added: Specification Clarifications: 4-GPIO25 Pull-up, 5-HPET TIMERn_32MODE_CNF, 6-PCI Clock, 7-Reserved Clarification.	April 20, 2005
11.0	Modified: Specification Clarifications: 5-HPET TIMERn_32MODE_CNF Added: Errata: 34-SATA AHCI Recovery From Task File Error Specification Clarifications: 8-PATA Secondary Command/Control BAR Documentation Changes: 5-IDE MSE Bit, 6-PxCMD.ST Bit Description Correction	May 18, 2005

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel® I/O Controller Hub 6 (ICH6) Family Datasheet	301473-002

Nomenclature

Errata are design defects or errors. Errata may cause the ICH6's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Intel® I/O Controller Hub 6 (ICH6) family. Intel intends to fix some of the errata in a future stepping of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Specification Change, Erratum, Specification Clarification or Documentation Change that applies to a stepping or to this product line.

(No mark) or
(Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc: Document change or update that will be implemented.

PlanFix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

Bar: This item is either new or modified from the previous version of the document.

Errata

Erratum Number	Stepping			Status	ERRATA
	B1	B2	C0		
1	X	X	X	No Fix	SATA COMINIT/COMWAKE Detection
2	X	X	X	No Fix	PCI Express* Common Mode Voltage Noise Immediately Following Receiver Detect Sequence
3	X			Fixed	SATA Swap Bay Device Detection
4	X	X	X	No Fix	Intel® ICH6 SATA Sending Less Than Minimum Number of PMACK
5	X	X	X	No Fix	Intel ICH6 Improper Length Register Device-to-Host FIS
6	X	X	X	No Fix	Intel ICH6 Split Lock LPC Cycle
7	X			Fixed	Intel ICH6 Completion Delays
8	X	X	X	No Fix	Intel ICH6 SATA Signal Voltage Level

Errata

Erratum Number	Stepping			Status	ERRATA
	B1	B2	C0		
9	X	X	X	No Fix	Intel ICH6 PCI Express* Completion Timer Not Halting in L1
10	X	X		Fixed	Intel ICH6 Does Not Send Minimum Number of TS2 on PCI Express*
11	X	X		Fixed (DT)	PCI Express* Recovery
12	X	X	X	No Fix	Intel ICH6 PCI Express* Extended Tag Capability Bit
13	X	X	X	No Fix	ICH6 Does Not Ignore a PCI Express Null Packet
14	X	X	X	No Fix	ICH6 PCI Express DLLPs with Unknown Encoding Type
15	X	X	X	No Fix	SATA SRST during Link Low Power States
16	X	X	X	No Fix	PCI Express Replay
17	X	X	X	No Fix	ICH6R SATA FIS Posting Cycle
18	X	X	X	No Fix	USB Output Voltage
19	X	X	X	No Fix	ICH6 AHCI Command FIS SYNC Escape
20	X	X	X	No Fix	ICH6 AHCI PxCMD.CR Bit
21	X	X	X	No Fix	ICH6 High Definition Audio Payload Capabilities Registers
22	X	X	X	No Fix	ICH6 PIO Setup FIS Error
23	X	X	X	No Fix	ICH6 PCI Express Suprise Removal
24	X	X	X	No Fix	PCI Express Scrambling
25	X	X	X	No Fix	AHCI PxSERR:[M] Bit
26	X	X	X	No Fix	L0s with Extended Sync
27	X	X	X	No Fix	ICH6-M DPRSLPVR
28	X	X	X	No Fix	PATA V- Threshold
29	X	X	X	No Fix	PCI Express SKP/InitFCx Contention
30	X	X	X	No Fix	DMI L0s Latency Bit Attribute
31	X	X	X	No Fix	PCI Express Two DWord Malformed TLP
32	X	X	X	No Fix	Full Speed USB ISOC End of Packet
33	X	X	X	No Fix	ICH6R/ICH6-M AHCI SATA Interlock Switch
34	X	X	X	No Fix	SATA AHCI Recovery From Task File Error

Specification Changes

Spec Change Number	Stepping			SPECIFICATION CHANGES
	B1	B2	C0	
				There are no specification changes in this specification update revision.

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
1	t216 Clarification
2	C2 Support
3	LPC Cycle Clarification
4	GPIO25 Pull-up
5	HPET TIMERn_32MODE_CNF
6	PCI Clock
7	Reserved Clarification
8	PATA Secondary Command/Control BAR

Documentation Changes

No.	DOCUMENTATION CHANGES
1	PCI Device Revision ID
2	CAP.SALP
3	Memory Address Range Addition
4	D30:F0 PSTS Correction
5	IDE MSE Bit
6	PxCMD.ST Bit Description Correction

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Identification Information

Markings

ICH6 Stepping	S-Spec	Top Marking	Notes
B1	N/A	82801FB QF88ES	Engineering Sample - ICH6
B1	SL7AG	82801FB SL7AG	Production ICH6
B1	N/A	82801FR QF89ES	Engineering Sample - ICH6R
B1	SL79N	82801FR SL79N	Production ICH6R
B1	N/A	82801FRW QF91ES	Not supported
B1	SL7LT	82801FRW SL7LT	Not supported
B1	N/A	82801FW QF92ES	Not supported
B1	SL7LM	82801FW SL7LM	Not supported
B2	N/A	82801FB QH16	Engineering Sample - ICH6
B2	N/A	82801FR QH17	Engineering Sample ICH6R
B2	N/A	82801FB QI29	Engineering Sample ICH6 (Lead Free)
B2	N/A	82801FBM QG87	Engineering Sample ICH6-M
B2	SL7W6	82801FBM SL7W6	Production ICH6-M
B2	N/A	82801FBM QH58	Engineering Sample ICH6-M (Lead Free)
B2	SL89K	82801FBM SL89K	Production ICH6-M (Lead Free)
B2	SL89L	82801FM SL89L	Production ICH6 (Lead Free)
B2	SL89J	82801FR SL89J	Production ICH6R (Lead Free)
B2	SL7Y5	82801FB SL7Y5	Production ICH6
B2	SL7W7	82801FR SL7W7	Production ICH6R
C0	N/A	82801FR QH82	Engineering Sample ICH6R
C0	N/A	82801FB QI08	Engineering Sample ICH6
C0	SL8BZ	82801FB SL8BZ	Production ICH6
C0	SL8C2	82801FR SL8C2	Production ICH6R

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Errata

1. SATA COMINIT/COMWAKE Detection

Problem: During Out-Of-Band (OOB) sequencing, the ICH6 may detect COMINIT/COMWAKE when only 2 or 3 bursts of ALIGNs are received from the SATA device instead of the required 4 bursts as per the SATA 1.0a Specification.

Implication: None Known - The ICH6 appropriately handles subsequent ALIGNs.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

2. PCI Express* Common Mode Voltage Noise Immediately Following Receiver Detect Sequence

Problem: The PCI Express common mode voltage is not stable immediately after Receiver Detect Sequence when entering Polling.Active from Detect.Active states.

Implication: Common mode voltage noise may result in bit errors early in Polling.Active state. This may result in additional training time before transitioning on to Polling.Configuration.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

3. SATA Swap Bay Device Detection

Problem: During non-AHCI SATA swap bay operation with slave device while master is present, slave device task file may stay at 00h if slave device not ready.

Implication: Slave SATA device swapped may not be detected.

Workaround: None.

Status: Fixed in B-2 stepping. For steppings affected, see the *Summary Tables of Changes*.

4. Intel® ICH6 SATA Sending Less Than Minimum Number of PMACK

Problem: The SATA Spec requires the ICH6 to send at least four PMACKs (Power Management Acknowledgments) to the SATA device. ICH6 sends only three PMACKs before entering a lower power state after the device requests partial or slumber state on the SATA bus.

Implication: None known. The SATA Specification intent is to provide four PMACK messages to provide redundancy thru repetition. the device is required to operate after receiving only one PMACK.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

5. Intel® ICH6 Improper Length Register Device-to-Host FIS

Problem: If a SATA device sends less than a 5 DWord Register Device-to-Host FIS, the ICH6 will correctly respond with RERR but may not be able to accept any further FISes from the device.

Implication: SATA bus will hang.

Note: This only applies while operating in AHCI mode.

Note: No known devices use Register Device-to-Host FIS sizes less than 5 DWords, as these are not allowed by the Serial ATA Specification, rev 1.0a.

Workaround: The AHCI driver shall reset the bus by sending COMRESET, per the AHCI spec.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

6. Intel® ICH6 Split Lock LPC Cycle

Problem: ICH6 may not properly complete non-DWord aligned locked cycles to LPC.

Implication: System Hang.

This issue has only been replicated using a synthetic test environment and has not been reported using commercially available hardware/software.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

7. Intel® ICH6 Completion Delays

Problem: ICH6 internal devices or devices connected to the ICH6 may experience additional completion delays of up to 40 usec.

Implication: No end user functional impact expected.

Most ICH6 devices are buffered adequately to withstand an additional 40 usec delay.

The UHCI (Full-speed only) may experience underruns and PCI may experience downstream request delays. Both implications are allowable their respective industry specifications.

Workaround: None.

Status: Fixed in B-2 stepping. For steppings affected, see the *Summary Tables of Changes*.

8. Intel® ICH6 SATA Signal Voltage Level

Problem: The ICH6 SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the ICH6 Serial ATA (SATA) transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications (section 6.6.2 of SATA Specification, rev 1.0a).

Implication: None known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

9. Intel® ICH6 PCI Express* Completion Timer Not Halting in L1

Problem: The ICH6 PCI Express* Completion Timer does not halt when the link enters the L1 state.

Implication: The ICH6 will flag a completion error:

Note that this requires a device that is not fully compliant with the PCI Express specification and has only been replicated in a synthetic test environment.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

10. Intel® ICH6 Does Not Send Minimum Number TS2 on PCI Express*

Problem: On PCI Express, the ICH6 transitions to Recovery.Idle after sending 9 TS2s (Training Order Sets) after receiving the first TS2 from the endpoint. The PCI Express specification requires that the ICH6 send a minimum of 16 TS2s after detecting the first TS2.

Implication: If the endpoint is unable to consecutively receive 8 of the 9 transmitted TS2s within 48 ms, the endpoint will transition to the Detect state and reattempt training. All known production devices have been able to properly train after receiving 9 TS2s.

Workaround: None.

Status: Fixed in C0. For steppings affected, see the *Summary Tables of Changes*.

11. PCI Express* Recovery

Problem: On PCI Express* L0s and L1 Exit, the ICH6 may fail to train to L0 and initiate Recovery.

Implication: ICH6 PCI Express interface times out during the Recovery state, which results in PCI Express link down conditions, sporadic recovery transitions, and possible system hangs.

Workaround: (Desktop) None necessary: L0s/L1 states are not enabled by the current desktop BIOS recommendations.

Workaround: (Mobile) BIOS Workaround. BIOS should do the following:

1. Ensure that bits [1:0] of Link Control register (D28:F0/F1/F2/F3:Offset 50h:[1:0] are 00b (power on default value) for all ICH6-M PCI Express root ports in the system.
2. In the ACPI_OSC control method, return the capabilities dword with bit-6 = 0 indicating that ASPM control should not be transferred to the OS with native PCI Express support.

Status: Fixed in C0 (Desktop). For steppings affected, see the *Summary Tables of Changes*.

12. Intel® ICH6 PCI Express* Extended Tag Capability Bit

Problem: The ICH6 incorrectly has the PCI Express Extended Tags Supported capability bit (D28:F0/F1/F2/F3:Offset 44h bit-5) set to ‘1’, though the ICH6 does not support Extended Tags.

Implication: Software will not be able to implement Extended Tags support.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

13. Intel® ICH6 Does Not Ignore a PCI Express* Null Packet

Problem: If the ICH6 receives a PCI Express Null packet, it should drop the packet and not perform sequence number checking or respond with any ACK or NAK DLLP. The ICH6 still performs sequence number checks for Null packets and may respond with an ACK or NAK depending on the result of the check.

Implication: ICH6 may send ACK or NAK DLLPs in response to a Null packet. This may degrade link performance due to unnecessary retries.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

14. Intel® ICH6 PCI Express* DLLPs with Unknown Type Encoding

Problem: If the ICH6 receives a DLLP on PCI Express with an unknown type encoding, the ICH6 may intrepret the packet as an ACK or NAK.

Implication: The ICH6 may intrepret the ACK as being from an outstanding TLP sent to the device, indicating that the device received the TLP. Or, the ICH6 may flag a DLLP protocol error if the sequence number is not appropriate. If the ICH6 intreprets the packet as a NAK, needless replay may occur.

Note: This requires PCI Express rev 1.0a and rev 1.1 noncompliant devices or require a future revision of the PCI Express spec to expand into currently undefined type encodings.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

15. SATA SRST during Link Low Power States

Problem: When exiting SATA link partial or slumber states, the ICH6 may not send a SRST when instructed by software.

Implication: The device will not appear available to software until SRST is re-tried.

Workaround: BIOS workaround available.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

16. PCI Express* Replay

Problem: The ICH6 PCI Express port's receiver does not properly recognize a ACK packet from a device when the ICH6 is replaying a packet.

Implication: PCI Express link may halt, resulting in a system hang.

This issue has only been replicated using a synthetic test environment using targeted error injection testing.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

17. Intel® ICH6R SATA FIS Posting Cycle

Problem: In only AHCI mode (ICH6R), the SATA controller may post a FIS incorrectly if either an unsolicited COMINIT arrives or if software performs a port reset, while FIS posting is pending internally.

Implication: Both a malformed TLP is delivered and inappropriate data is delivered on the next upstream cycle.

Note: This has only been replicated in a synthetic test environment and has not been reproduced in a real world environment.

Workaround: None. The system can be configured to detect this anomalous condition and reset the system to prevent this data migration. Refer to the ICH6 BIOS Specification for implementation details.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

18. USB Output Voltage

Problem: ICH6 High Speed USB2.0 V_{HSOL} and V_{HSOH} may not meet the USB 2.0 specification.

The maximum expected V_{HSOL} is 60 mV and the maximum expected V_{HSOH} is 470 mV.

Implication: None known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

19. Intel® ICH6 AHCI Command FIS SYNC Escape

Problem: If the ICH6 SATA controller is operating in AHCI mode and a device sends a SYNC escape, the ICH6 retries the Command FIS (CFIS) sent to the device. The SATA spec requires that the ICH6 not resend the CFIS.

Implication: The ICH6 may continuously retry until reset by software.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

20. Intel® ICH6 AHCI PxCMD.CR Bit

Problem: If a Task File fatal error occurs during a SATA AHCI transfer, the ICH6 will not automatically clear the PxCMD.CR bit, as required by the AHCI 1.0 spec, until the AHCI driver software follows the spec-defined recovery mechanism.

Implication: None known, as AHCI compliant driver software will cause the ICH6 to clear the CR bit during error recovery.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

21. Intel® ICH6 High Definition Audio Payload Capabilities Registers

Problem: The ICH6 High Definition Audio controller does not implement the OUTSTRMPAY and INSTRMPAY registers, per HD Audio spec rev 1.0.

Implication: None - the ICH6 supports all standard audio useage models. Additionally, HD Audio codecs do not support configurations that exceed the stream BW of the ICH6. However, if software programs the audio stream to a non-standard audio format that exceeds the bandwidth capabilities of the ICH6, then the stream's DMA engine may halt.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

22. Intel® ICH6 PIO Setup FIS Error

Problem: The ICH6 SATA AHCI controller may set the ERR.T and PxIS.IFS bits when a link error (such as a CRC error) or ICH6 SATA receiver error occurs on a PIO Setup FIS, instead of setting the PxIS.INFS bit, as defined by the AHCI 1.0 specification.

Implication: A spurious interrupt is generated and the AHCI driver software will detect the error and retry.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

23. Intel® ICH6 PCI Express* Surprise Removal

Problem: After eight surprise removal or non-software initiated link down events on a PCI Express port without a platform reset, the ICH6 may not be able to receive completions from the device on the PCI Express link.

Implication: System may hang.

Note: Issue requires multiple PCI Express devices to be populated in the system with simultaneous upstream requests. Software must also deprogram the PCI Express port number that experienced the event before hardware is able to fully respond to the link down condition. Known software does not deprogram surprise removal port before hardware responds. This issue has only been observed in a simulation environment.

Workaround: Perform platform reset.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

24. PCI Express* Scrambling

Problem: While entering the Recovery state, the ICH6 stops scrambling two symbols before the first TS (training sequence).

Implication: When these non-scrambled symbols are received by the endpoint, the de-scrambler of the endpoint will observe two symbols of random data. The first symbol of TS1 will reset the endpoint's de-scrambler so that the endpoint should recognize the TS1 and TS2 ordered-sets being transmitted and move into the Recovery state as planned.

There is no system level impact if the endpoint is PCI Express Specification 1.0a compliant in ignoring the random data.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

25. AHCI PxSERR:[M] Bit

Problem: The SATA AHCI controller incorrectly sets the PxSERR:[M] (Recovered Communications Error) bit if PhyRDY is established and either an internal overflow occurs or a miss-align (when SATA primitives are not detected on the correct primitive boundaries) occurs during resume from Partial/Slumber power management states.

Implication: The controller will set the PxIS:[INFS] bit which is informative only and is recoverable by software. There is no impact to system operation.

Workaround: None needed.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

26. L0s With Extended Sync

Problem: If Extended Sync and L0s are both enabled, the ICH6 may lose proper sequence of ACK messages when the link is resuming from L0s.

Implication: System may hang.

Extended Synch mode only intended for debug and test environment.

Note: This impacts both DMI and PCI Express.

Workaround: None

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

27. ICH6-M DPRSLPVR

Problem: The DPRSLPVR signal may not be properly initialized until ICH6-M's core well power rails (Vcc1_5, Vcc3_3) become stable and ICH6-M receives PCI clock.

Implication: The system may fail to boot depending on the power sequencing logic implementation and CPU VR solution used on the platform.

Workaround: An external weak pull-down resistor of 100K ohms will ensure DPRSLPVR does not float on affected systems.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

28. PATA V- Threshold

Problem: The ICH6 may violate the $V\text{-}_{min}$ spec, per the AT Attachment with Packet Interface - 7 specification.

Implication: None known. Intel has performed extensive, targeted validation without any detected functional issues.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

29. PCI Express* SKP/InitFCx Contention

Problem: During ICH6 PCI Express initialization, if a SKP is being transmitted immediately before a InitFCx DLLP, then a partial InitFCx may be transmitted.

Implication: A slight delay (less than 100 ns) may occur during link initialization. Device may report correctable errors. InitFCx will automatically be repeated.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

30. DMI L0s Latency Bit Attribute

Problem: ICH6 DMI L0s exit latency bits (RCRB+1A4h, bits 14:12) are Read/Write, not Read Only.

Implication: None known. Software should not write to this register.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

31. PCI Express* Two DWord Malformed TLP

Problem: If the ICH6 receives a two DWord TLP (which is not legal per PCI Express Spec), the ICH6 may flag the immediately following TLP as malformed.

Implication: Incorrectable error flagged and system may hang.

This issue has only been replicated using a synthetic test environment with an illegal 2 DWord TLP injected onto the PCI Express bus and has not been reported using commercially available hardware/software.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

32. Full speed USB ISOC End of Packet

Problem: If a Full-speed USB ISOC OUT transaction occurs very late in the USB frame such that the payload cannot be contained in that frame, then a bit stuff error is created as defined in the USB 2.0 specification and flagged to both host software and device. When this occurs, and a specific data pattern is present, then the End of Packet (EOP) will not be sent. In this event, devices attached to that UHCI controller may not detect the subsequent Start of Frame (SOF) due to lack of EOP.

Implication: None, the resulting bit stuff error and device not detecting SOF are recoverable events by USB 2.0 system design.

Note: USB ISOC traffic and SOF packets are not necessarily data coherent by definition of the protocol. This issue has only been replicated in a synthetic test environment and has not been reproduced in known system configurations.

Workaround: None.

Status: No Fix.

33. AHCI SATA Interlock Switch

Problem: In AHCI enabled systems using the native interlock switch for Hot Plug, the PxIS:[DIS] bit in D31:F2 may not reflect the change in connection of a SATA device on a port via the SATA[n]GP§ pin.

Implication: The SATA controller may not properly detect a device insertion or removal event possibly resulting in loss of unsaved data (for removals), or failure to detect device presence (for insertions).

Workaround: This applies only to platforms implementing Hot Plug via an interlock switch using SATA[n]GP signals. For systems that do not have Hot Plug capability, or that do not use SATA[n]GP, no workaround is needed.

- Either completely disable all Hot Plug support by
  - Clearing CAP:[SIS (bit-28)], PxCMD:[HPCP (bit-18)] and PxCMD:[ISP (bit-19)]

OR

- Use a GPI instead of the SATA[n]GP signal following these steps:
  - Completely disable all Hot Plug support as indicated above and
  - Use an SCI/SMI capable GPI(15:0) routed to the HDD interlock switch.

Status: No Fix.

34. SATA AHCI Recovery From Task File Error

Problem: During an AHCI fatal error condition, if the device signals a Task File Error (TFES), the ICH6 may not be able to recover correctly after software performs the AHCI spec-defined fatal error recovery mechanism.

Implication: SATA port will appear bus resulting in the device being inaccessible.

Note: IAA/IAMT 4.0 and later implements a reset mechanism that does not allow this issue to be exposed.

Workaround: AHCI driver should toggle the ST bit to ‘1’ and back to ‘0’ upon detecting TFES bit set after ST bit is cleared.

Status: No Fix.

§

Specification Changes

There are no Specification Changes in this Specification Update revision.

§

Specification Clarifications

1. t216 Clarification

Note 10 is added to parameter t216 (Table 22-21 (Power Sequencing and Reset Signal Timings)

Note 10: Vcc3)3 should be used for DPRSLPVR, STP_PCI#, STP_CPU# and V_CPU_IO should be used for STPCLK#, CPUSLP#, DPSLP#, DPRSTP#.

2. C2 Support

C2 support is provided for only in the ICH6-M. The title of section 10.8.3.6 is changed to "LV2 - Level 2 Register (Mobile Only)"

The first two rows of Table 5-25 State Transition Rules for Intel ICH6 are changed as indicated below:

Present State	Transition Trigger	Next State
G0/S0/C0	• Processor halt instruction • Level 2 Read (Mobile Only) • Level 3 Read (Mobile Only) • Level 4 Read (Mobile Only) • SLP_EN bit set • Power Button Override • Mechanical Off/Power Failure	• G0/S0/C1 • G0/S0/C2 • G0/S0/C2, G0/S0/C3 or G0/S0/C4 - depending on C4onC3_EN bit (D31:F0;Offset A0h:bit-7 and BM_STS_ZERO_EN bit (D31:F0;Offset A9h:bit-2) (Mobile Only) • G1/Sx or G3/S5 state • G2/S5 • G3
G0/S0/C1	• Any Enabled Break Event • STPCLK# goes active • Power Button Override • Power Failure	• G0/S0/C0 • G0/S0 / C2 (Mobile Only) • G2/S5 • G3

3. LPC Cycle Clarification

The following changes are made to Table 5-4 LPC Cycle Types Supported in section 5.5.1.1:

- "See Note 1" is removed from the comment column for both I/O Read and I/O Write cycle types.§
- "See Note 1 is added to the comment column for both Memory Read and Memory Write cycle types.
- Note 1 is replaced with the following text:

"For memory cycles below 16MB that do not target enabled firmware hub ranges, the ICH6 performs standard LPC memory cycles. It only attempts 8-bit transfers. For larger transfers, ICH6 performs multiple 8-bit transfers. If the cycle is not claimed by any peripherals, it is

subsequently aborted, and the ICH6 returns a value of all 1s to the processor. This is done to maintain compatibility with ISA memory cycles where pull-up resistors would keep the bus high if no device responds."

4. GPIO25 Pull-up

Table 3-1 incorrectly applies Note 11 to the GPIO[25] signal. This reference to Note 11 is removed for GPIO[25].

5. HPET TIMERn_32MODE_CNF

The description of TIMERn_32MODE_CNF (section 20.1.5) is replaced as follows:

Bit	Description
8	Timer n 32-bit Mode (TIMERn_32MODE_CNF) - R/W or RO. Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if software is not willing to halt the main counter to read or write a particular timer, and the software is not capable of atomic 64-bit operations to the timer. This bit is only relevant if the timer is operating in 64-bit mode in which case that timer can be forced to 32-bit mode by setting this bit. When Timer 0 is switched to 32-bit mode, the upper 32 bits are loaded with all 0's which will remain when the timer is switched back to 64-bit mode. If the timer is not in 64-bit mode, then this bit will always be read as 0 and writes will have no effect. Timer 0: Read/Write (default 0). 0 = 64-bit, 1=32-bit. Timers 1/2: Hardwired to 0. Writes have no effect since these timers are 32-bit only.

6. PCI Clock

The ICH6 PCI was designed to meet the requirements for the PCI 2.3 specification. As a result, Table 22-9 is updated to match that specification using the below table.

Sym	Parameter	Min.	Max	Unit	Figure	Notes
PCI Clock (PCICLK)						
t1	Period	30	33.3	ns	22-1	
t2	High Time	11		ns	22-1	
t3	Low Time	11		ns	22-1	
t4	Rise Time	1	4	V/ns	22-1	
t5	Fall Time	1	4	V/ns	22-1	

7. Reserved Clarification

The following text is added to the bottom of Chapter 6 (before section 6.1):

"All bit(s) or bit-fields listed as Reserved must be correctly dealt with by software. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit locations are preserved. Any ICH6 configuration register or I/O or memory mapped location not explicitly indicated in this document must be considered reserved."§

8. PATA Secondary Command/Control BAR

The following sentence is added to the descriptions of the Base Address field for both SCMD_BAR and SCNL_BAR (sections 11.1.13 and 11.1.14):

“This must not be programmed below 100h”

§

Document Changes

1. PCI Device Revision ID

PCI Revision ID Register values (PCI Offset 08h) for all ICH6 functions are shown below. This information is not found in the datasheet. This is the standard reference document.

Device Function	Description	Intel® ICH6 Dev ID	ICH6 B1 Rev ID	ICH6 B2 Rev ID	ICH6 C0 Rev ID	Comments
D31, F0	LPC	2640h	03h	04h	05h	ICH6/ICH6R
		2641h	03h	04h	N/A	ICH6-M
D31, F1	IDE	266Fh	03h	04h	05h	
D31, F2 SATA		2651h	03h	04h	05h	ICH6
		2652h	03h	04h	05h	ICH6R
		2653h	03h	04h	N/A	ICH6-M
D31, F3	SMBus	266Ah	03h	04h	05h	
D30, F0	DMI to PCI Bridge	244Eh	D3h	D4h	D5h	
		2448h	D3h	D4h	N/A	ICH6-M
D30, F2	AC '97 Audio	266Eh	03h	04h	05h	
D30, F3	AC '97 Modem	266Dh	03h	04h	05h	
D29, F0	USB UHC #1	2658h	03h	04h	05h	
D29, F1	USB UHC #2	2659h	03h	04h	05h	
D29, F2	USB UHC #3	265Ah	03h	04h	05h	
D29, F3	USB UHC #4	265Bh	03h	04h	05h	
D29, F7	USB EHCI	265Ch	03h	04h	05h	
D28:F0	PCI Express* Port 1	2660h	03h	04h	05h	
D28:F1	PCI Express Port 2	2662h	03h	04h	05h	
D28:F2	PCI Express Port 3	2664h	03h	04h	05h	
D28:F3	PCI Express Port 4	2666h	03h	04h	05h	
D27:F0	Intel® High Definition Audio	2668h	03h	04h	05h	
D8:F0	LAN	1065h[1]	03h	04h	05h	

NOTES:
1. Loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the device ID location, then 266Ch is used. Refer to the ICH6 EEPROM Map and Programming Guide for LAN Device IDs.

NOTE:
1. VccRTC at 3.0 V while the system is in G3 state at room temperature and only the G3 state for this power well is shown to provide an estimate of battery life.

2. CAP.SALP

Section 12.3.1.1 (CAP - Host Capabilities Register) incorrectly identifies the attribute for its SALP (bit-26) bit. It is changed to R/WO.

3. Memory Address Range Addition

Section 6.4, the following row is added to Table 6-4:

Memory Range	Target	Dependency/Comments
FED4 0000h - FED4 0FFFh	TPM on LPC	

4. D30:F0 PSTS Correction

In section 9.1.4, D30:F0;PSTS, the description for bit-0 is change to Reserved.

5. IDE MSE Bit

In section 11.1.3 (PCI Command Register) the description for bit-1 is incorrect and is changed to the following:

Bit	Description
1	**Memory Space Enable (MSE)** - RO

6. PxCMD.ST Bit Description Correction

The description for the Start bit in PxCMD (section 12.3.2.7) incorrectly refers to section 12.2.1 of the Serial ATA AHCI Specification. This is corrected to section 10.3.1.